Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 096032B-W

Product Specification ***Version : 02***

25.05.2009

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2009/03/02	SPEC.
02	CHANGE PIN LAYOUT	2009/05/25	MH

C O N T E N T S

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	96x32	dots
Module dimension (L*W*H)	28.5*11.5*1.41(MAX)	mm
Active area	19.18*6.38	mm
Dot size	0.18(W)X0.18(H)	mm
Dot pitch	0.20(W)X0.20 (H)	mm
Color	White	

(2) Controller IC: SSD1307 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Humidity		—	—	85	%
Supply Voltage For Logic	VDD	-0.3	—	4	V
Supply Voltage For Panel	Vcc	7	—	16	V
Operating lifetime			30,000(*)		Hrs

*:100cd/m^2 light on

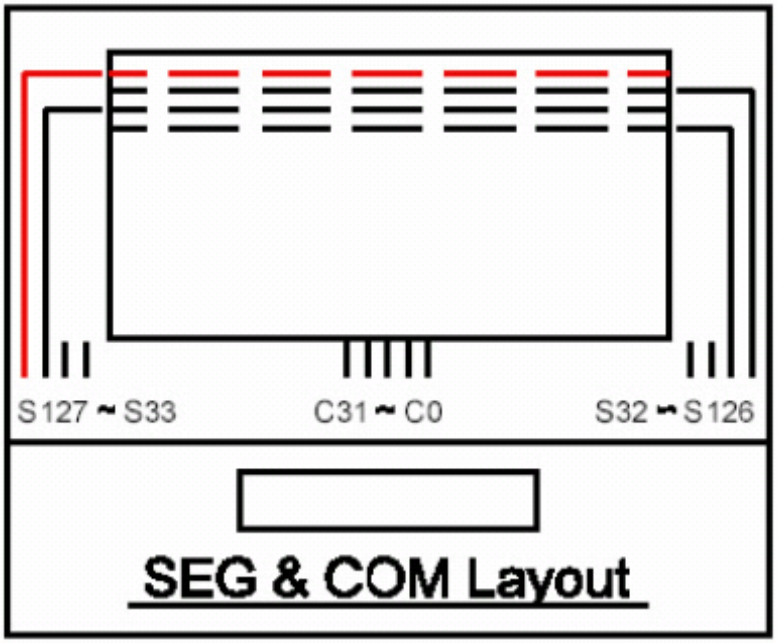
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	1.65	2.8	3.3	V
Supply Voltage For Panel	Vcc-V_{SS}	—	11.5	12	12.5	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	—	V
Input Low Vol	V_{IL}	—	—	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	—	V
Output Low Vol.	V_{OL}	—	—	—	0.1V_{DD}	V
Supply Current For Logic	I_{DD}	All pixels on	—	5	6	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

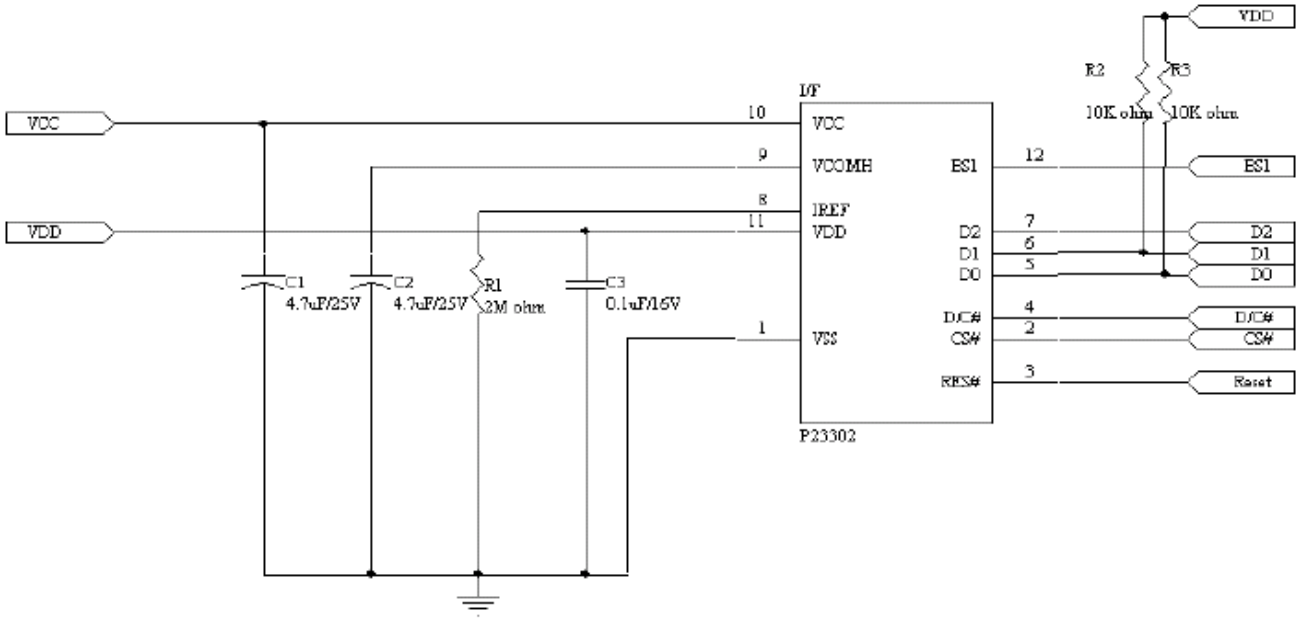
6. Panel Layout Diagram



7. Interface Pin Function

Pin No.	Symbol	Description
1	VSS	This is a ground pin.
2	CS	This pin is the chip select input.
3	RES	Hardware reset signal
4	D/C	In 4-wire Serial mode, this is Data/Command control pin. In I2C mode, this pin acts as SA0 for slave address selection.
5	D0	4-wire SPI: SCLK I2C: SCL
6	D1	4-wire SPI: SDIN I2C: SDAIN
7	D2	4-wire SPI: NC I2C: SDAOUT
8	IREF	The current reference input pin, this pin should be connected to ground through a resistor
9	VCOMH	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
10	VCC	Positive OLED high voltage power supply
11	VDD	Power supply for logic circuit
12	BS1	MCU Bus Interface Pin Selection 0: 4-wire Serial Interface 1: I2C Interface

8. Power Supply For LCD Module



Component：

C1、C2：4.7uF/16V(0805)

C3：0.1uF/16V(0603)

R1：2M ohm 1%(0603)

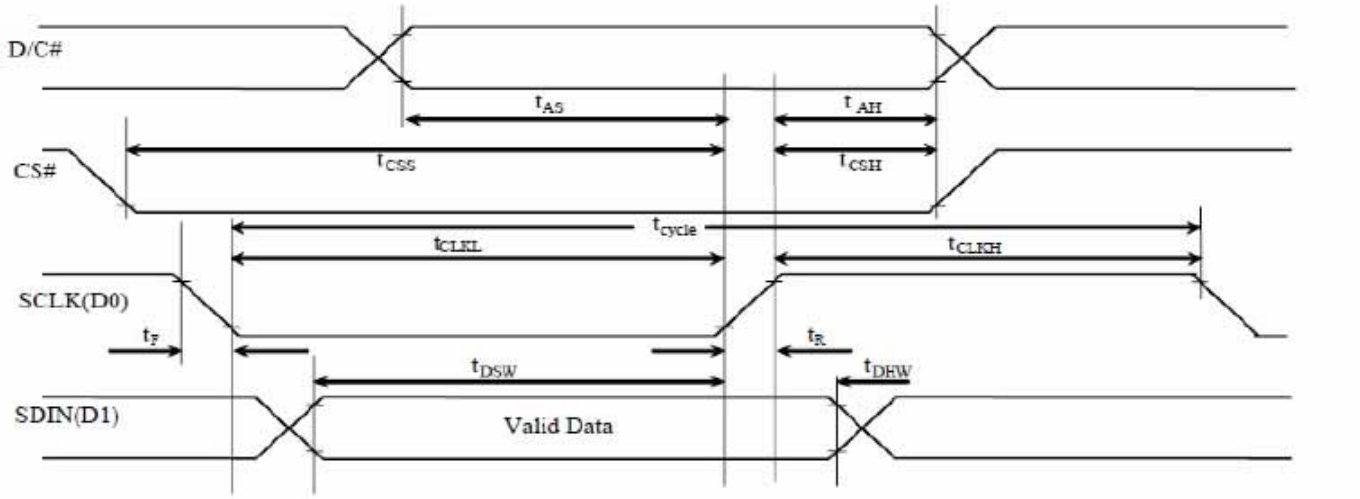
R2、R3：10K ohm (0603)

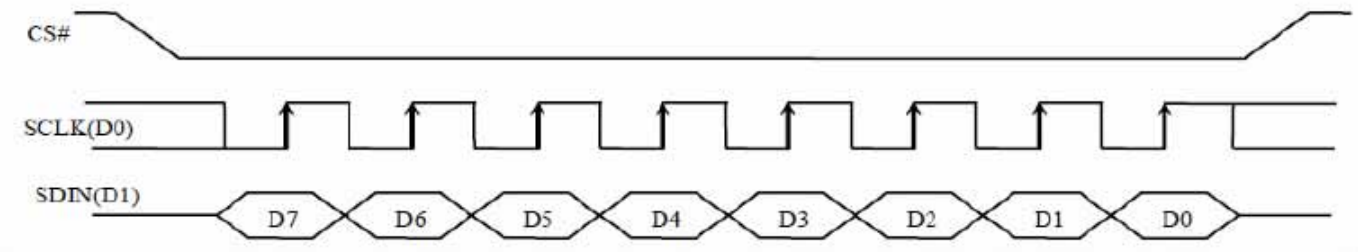
This circuit is for I^2C Interface

9. Timing Characteristics

9-1.SPI Interface

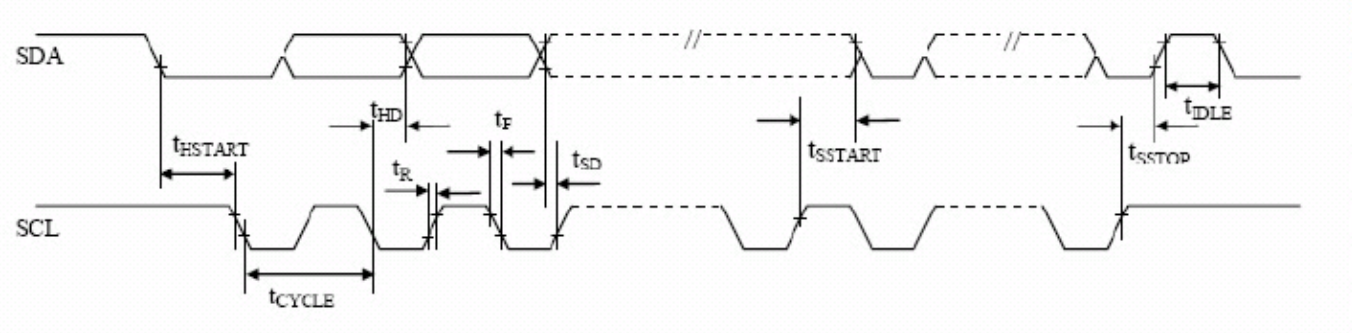
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns





9-2.I2C Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

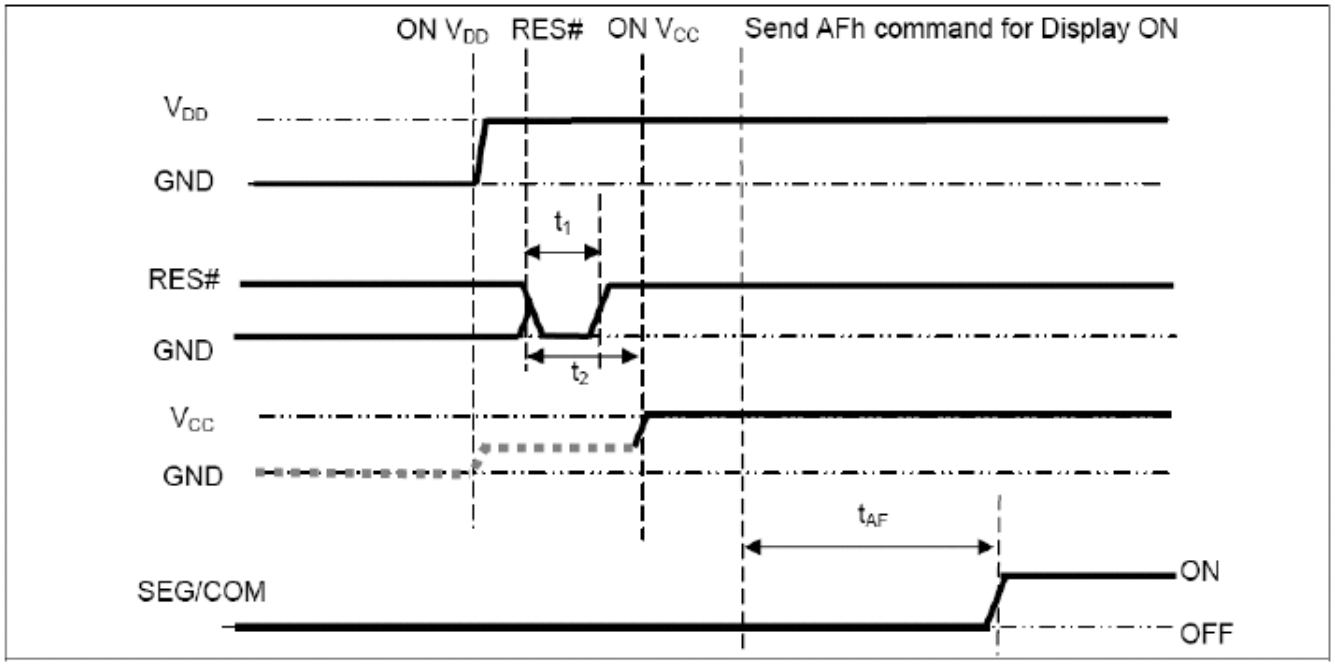


10. Power ON / OFF Sequence & Application Circuit

10.1 POWER ON / OFF SEQUENCE

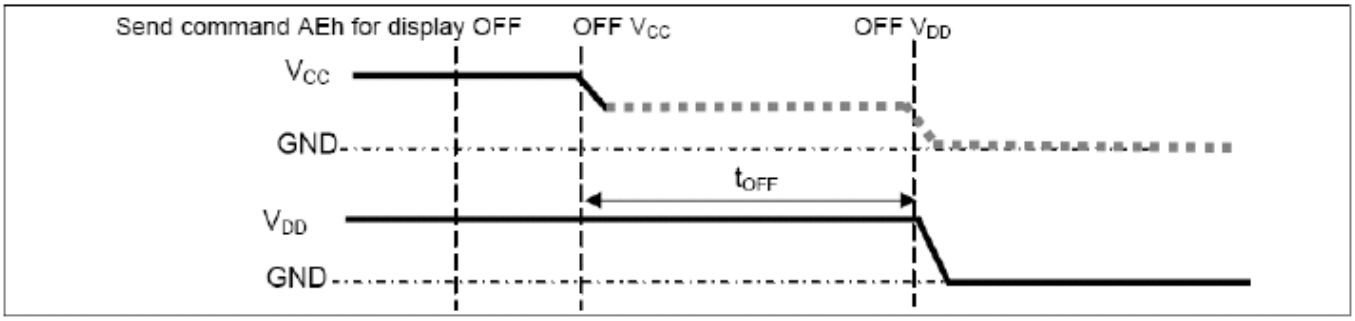
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM wil be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VDD and VCC,VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2)VCC should be disabled when it is OFF.

11. GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed.

The size of the RAM is 128 x 39 bits and the RAM is divided into five pages, from PAGE0 to PAGE4, which are used for monochrome 128x39 dot matrix display, as shown in below figures.

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row. For PAGE4, bit D7 is treated as don't care bit.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

GDDRAM pages structure of SSD1307

Segment re-mapping (command A1h)		SEG127	SEG126	SEG125	SEG124	.....	SEG4	SEG3	SEG2	SEG1	SEG0		
Segment re-mapping (command A0h [RESET])		SEG0	SEG1	SEG2	SEG3	.....	SEG123	SEG124	SEG125	SEG126	SEG127		
Page	Data	COL0	COL1	COL2	COL3	.....	COL123	COL124	COL125	COL126	COL127	COM Output Scan Direction (command C0h [RESET])	COM Output Scan Direction (command C8h)
0	D0					.....						COM0	COM38
	D1											COM1	COM37
	D2											COM2	COM36
	D3											COM3	COM35
	D4											COM4	COM34
	D5											COM5	COM33
	D6											COM6	COM32
	D7											COM7	COM31
1	D0					.....						COM8	COM30
	D1											COM9	COM29
	D2											COM10	COM28
	D3											COM11	COM27
	D4											COM12	COM26
	D5											COM13	COM25
	D6											COM14	COM24
	D7											COM15	COM23
2	D0					.....						COM16	COM22
	D1											COM17	COM21
	D2											COM18	COM20
	D3											COM19	COM19
	D4											COM20	COM18
	D5											COM21	COM17
	D6											COM22	COM16
	D7											COM23	COM15
3	D0					.....						COM24	COM14
	D1											COM25	COM13
	D2											COM26	COM12
	D3											COM27	COM11
	D4											COM28	COM10
	D5											COM29	COM9
	D6											COM30	COM8
	D7											COM31	COM7
4	D0					.....						COM32	COM6
	D1											COM33	COM5
	D2											COM34	COM4
	D3											COM35	COM3
	D4											COM36	COM2
	D5											COM37	COM1
	D6											COM38	COM0
	D7	Don't care bit											

Each box represents one bit of image data

12. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and faces Cycles: 1	——
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	——

13. Appendix (Drawing)