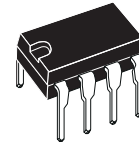




TV EAST/WEST CORRECTION CIRCUIT

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT
- EXTERNAL KEYSTONE ADJUSTMENT (symmetry of the parabola)
- INPUT FOR DYNAMIC FIELD CORRECTION (beam current change)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY RE-DELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAWTOOTH



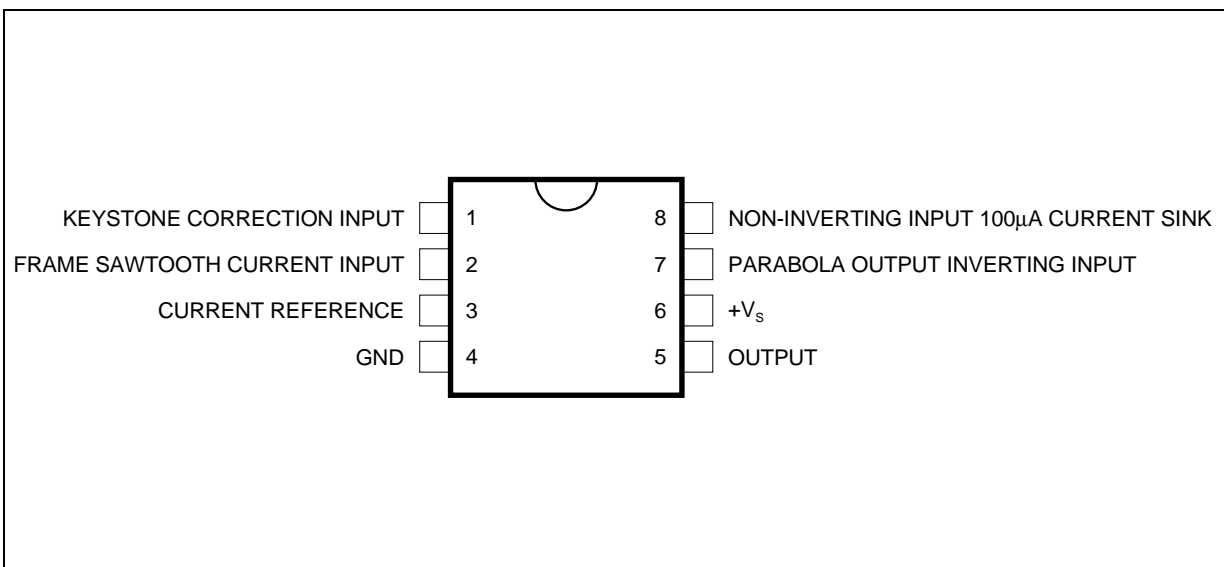
POWERDIP8 (Th = 0.4mm)
(Plastic Package)

ORDER CODE : TDA4950

DESCRIPTION

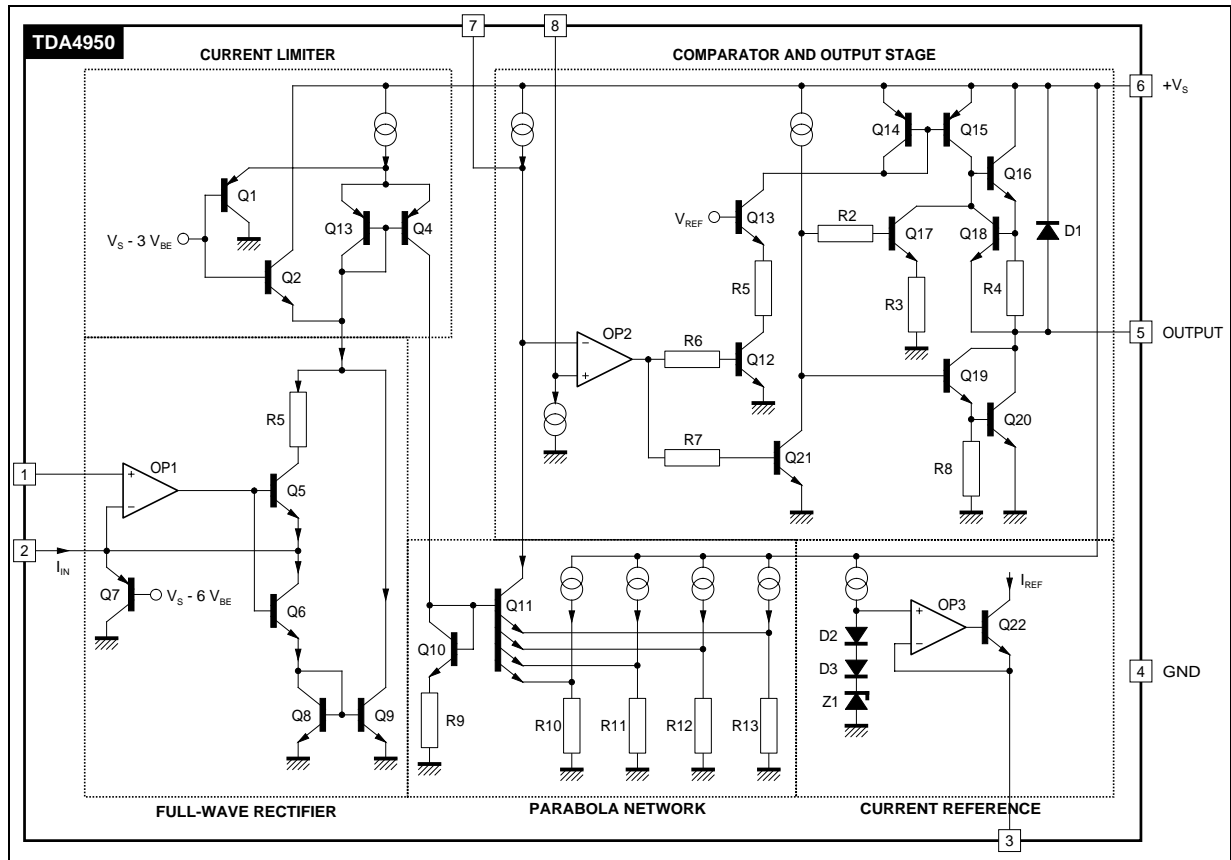
The TDA4950 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

PIN CONNECTIONS



495001EPS

BLOCK DIAGRAM



4950-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
I_S	Supply Current	500	mA
P_{tot}	Power Dissipation at $T_{amb} = 70^\circ\text{C}$	800	mW
T_{stg}, T_j	Storage and Junction Temperature	- 25, +150	$^\circ\text{C}$

4950-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Thermal Resistance Junction-ambient	Max. 100	$^\circ\text{C/W}$
$R_{th(j-c)}$	Thermal Resistance Junction-pin (4)	Max. 70	$^\circ\text{C/W}$

4950-02.TBL

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$, $V_S = 26\text{ V}$, $V_{fr} = 0$, S1 and S2 in "a" position, refer to test circuit unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		17	24	30	V
I_S	Supply Current			4.5	7	mA
V_{ref}	Internal Reference Voltage		7.6	8.0	8.8	V
$-I_{ref}$	Internal Reference Current	$V_{ref}/R3$		0.73		mA
$V_{7(A)}$	Pin 7 Output Voltage	$I_{fr} = 0\ \mu\text{A}$, see Figure 2	15.3	16.0	16.7	V
$V_{7(B)}$	Pin 7 Output Voltage	$I_{fr} = 30\ \mu\text{A}$, see Figure 2		15		V

4950-03.TBL

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$, $V_S = 26 V$, $V_{fr} = 0$, S1 and S2 in "a" position, refer to test circuit unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K1	Parabola Coefficient	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$, see Figure 2		0.28		
K2	Parabola Coefficient	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$, see Figure 2		0.71		
ΔV_7 (*)		$\Delta V_7 = V_{7E} - V_{7F}$, see Figure 2	- 40		40	mV
I_B	Current Source	S1 \rightarrow b		100		μA
V_{SATL}	Saturation Voltage	$I_o = 400 mA$ Sink S2 \rightarrow b		1	2	V
V_{SATH}	Saturation Voltage	$I_o = 100 mA$ Source S2 \rightarrow c S1 \rightarrow b		0.8	1.5	V
V_F	Forward Voltage	$I_o = 400 mA$ S2 \rightarrow d S1 \rightarrow b		1.2	1.7	V
I_{fr}	Frame Sawtooth Current	$V_{fr} = 6.6 V_{PP}$		66		μA

Figure 1 : Test Circuit

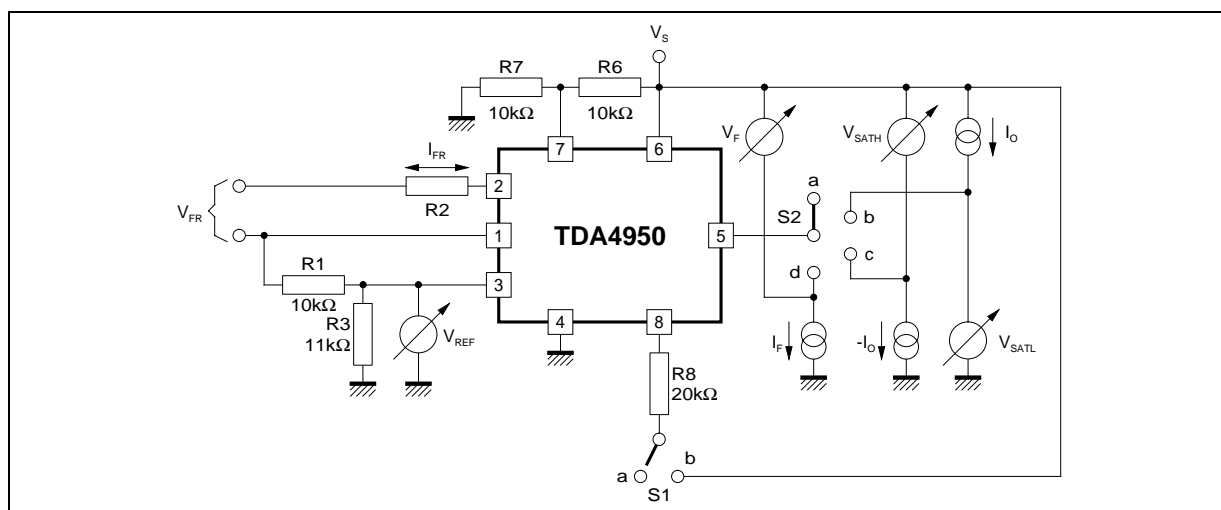
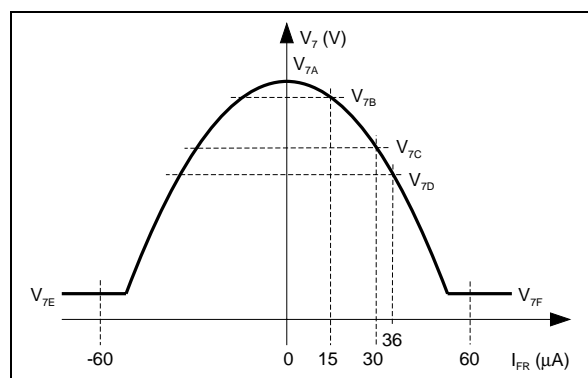


Figure 2 : Parabola Characteristics



CIRCUIT OPERATION

(see the schematic diagram)

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of $\pm 33\mu A$ which is produced via an external resistor from the sawtooth voltage. The non-inverting input of this amplifier is connected with a reference voltage corresponding

to the DC level of the sawtooth voltage. This DC voltage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current. This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

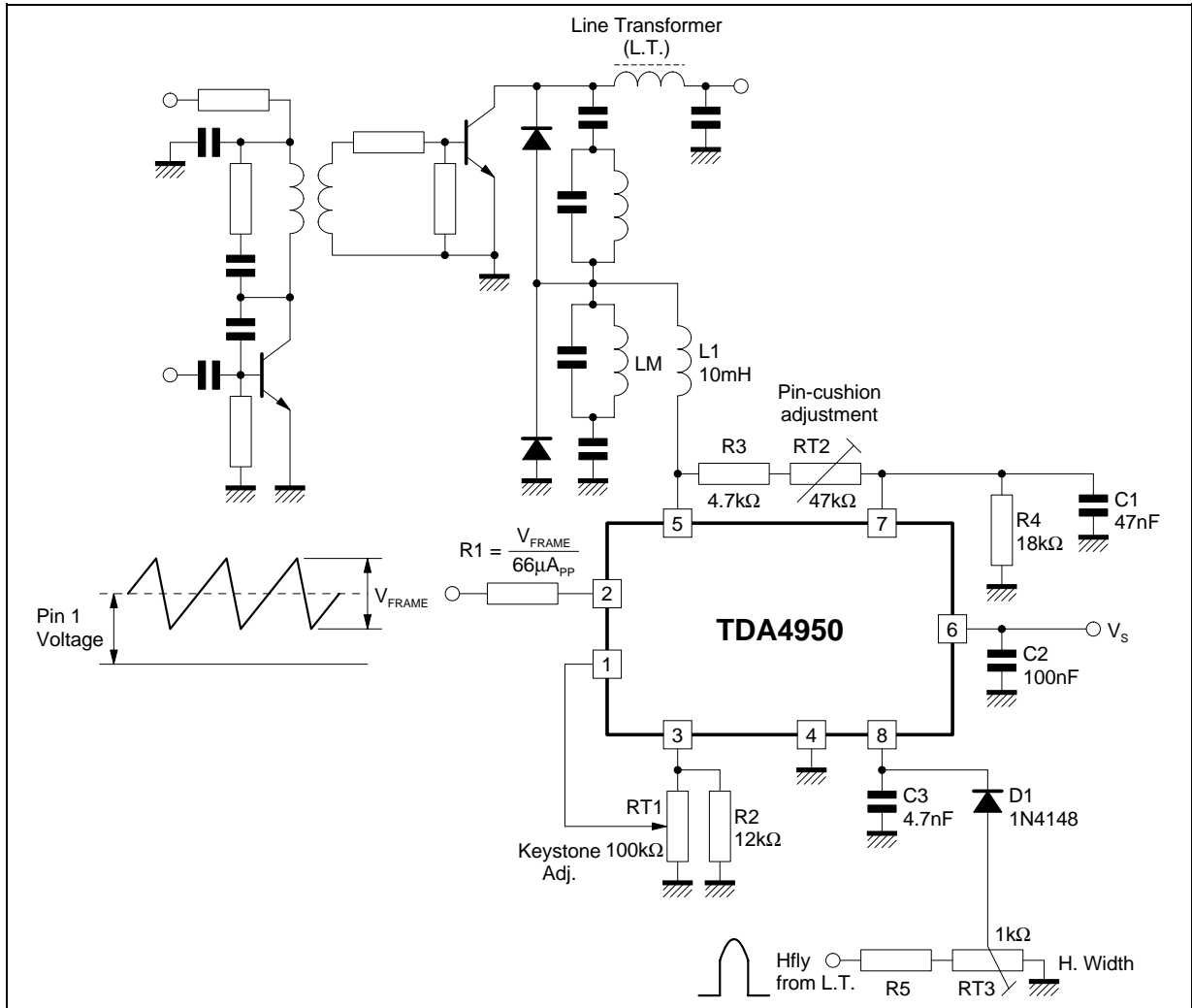
If the input is overmodulated ($> 40\mu A$) the internal current is limited to $40\mu A$. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

The horizontal frequency pulse-width modulated output signal drives the final stage. It consists of a class D push-pull output amplifier that drives, via an external inductor, the diode modulator.

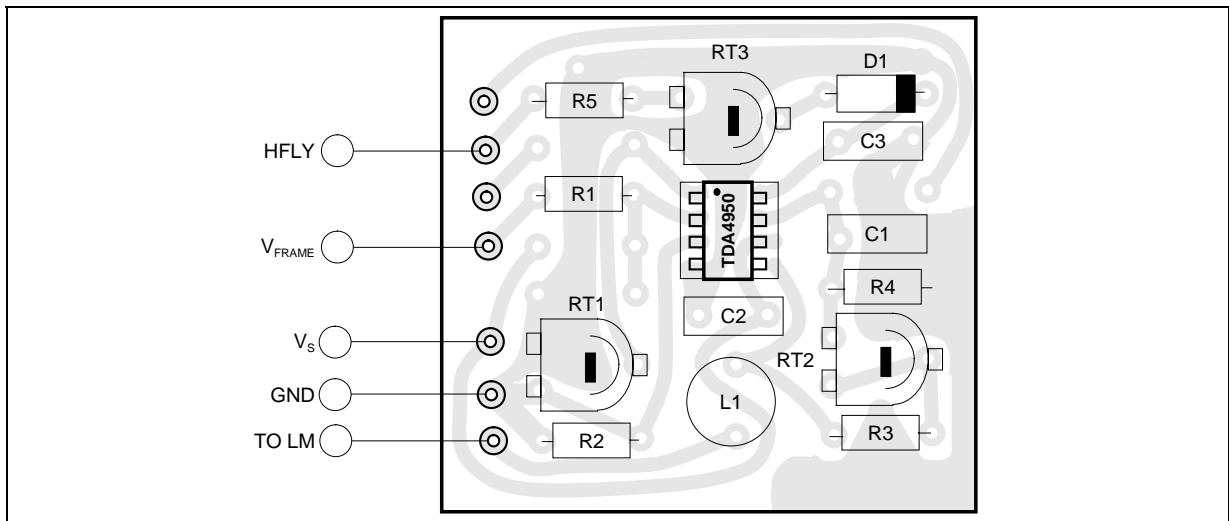


Figure 3 : Application Circuit with Keystone Correction

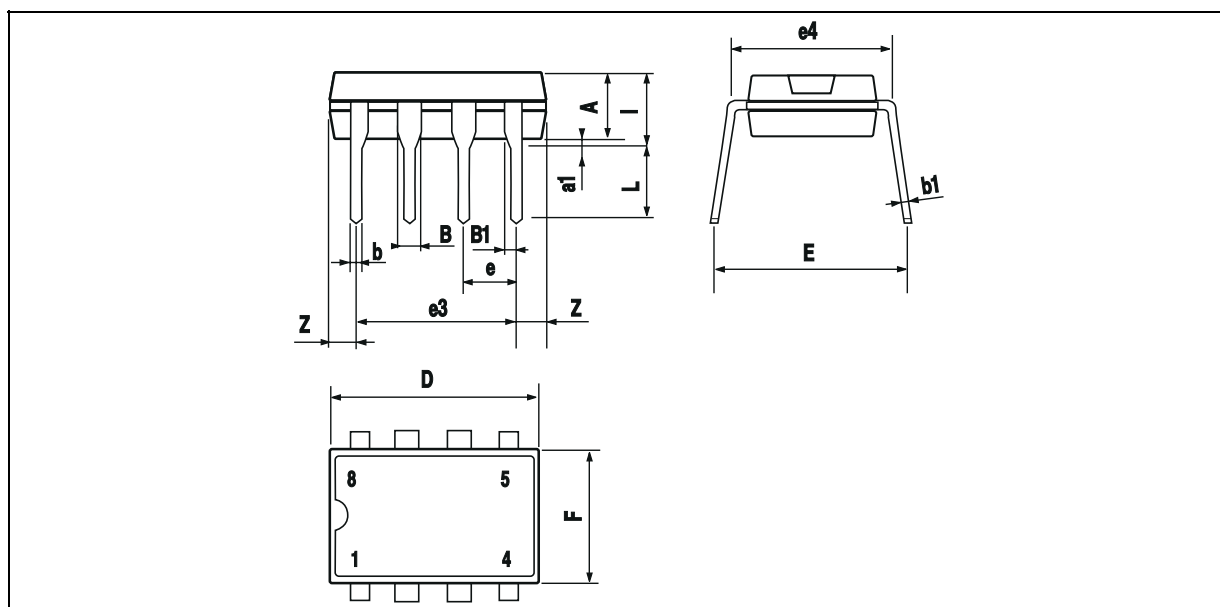


4950-05.EPS

Figure 4 : P.C. Board and Component Layout of the Circuit of Figure 3 (1:1 scale)



4950-06.EPS

PACKAGE MECHANICAL DATA
 8 PINS - PLASTIC POWERDIP


PM-DIP8EFS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.020		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

DIP8PW.TEL

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