SCLS039C - DECEMBER 1982 - REVISED MAY 1997

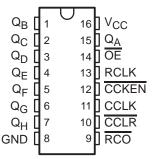
- 8-Bit Counter With Register
- High-Current 3-State Parallel Register
   Outputs Can Drive up to 15 LSTTL Loads
- Counter Has Direct Clear
- Package Options Include Plastic Small-Outline (D, DW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

#### description

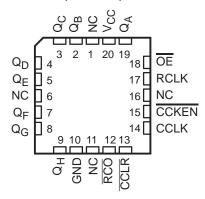
The 'HC590A contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ( $\overline{CCLR}$ ) and count-enable ( $\overline{CCKEN}$ ) inputs. A ripple-carry output ( $\overline{RCO}$ ) is provided for cascading. Expansion is easily accomplished for two stages by connecting  $\overline{RCO}$  of the first stage to  $\overline{CCKEN}$  of the second stage. Cascading for larger count chains can be accomplished by connecting  $\overline{RCO}$  of each stage to the counter clock ( $\overline{CCLK}$ ) input of the following stage.

Both CCLK and the register clock (RCLK) input are positive-edge triggered. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

SN54HC590A . . . J OR W PACKAGE SN74HC590A . . . D, DW, OR N PACKAGE (TOP VIEW)



SN54HC590A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN54HC590A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC590A is characterized for operation from –40°C to 85°C.

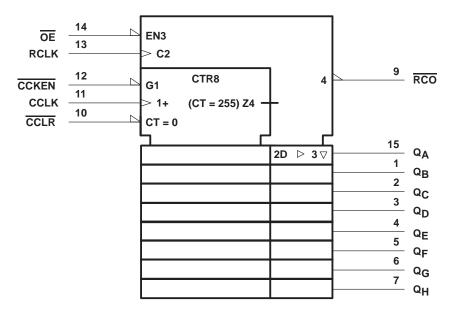


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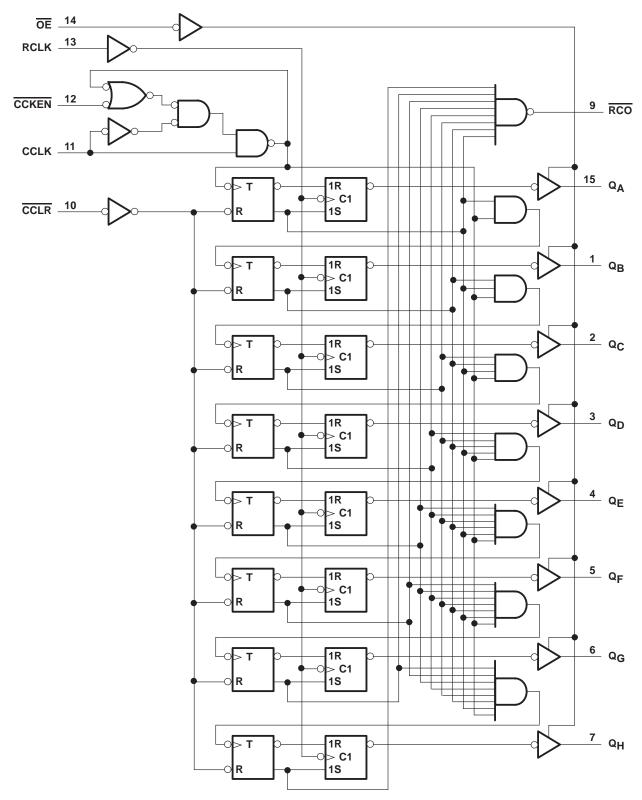
# logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DW, J, N, and W packages.



### logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.



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### absolute maximum ratings over operating free-air temperature range

Supply voltage range, V <sub>CC</sub>		0.5	V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see			
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CO</sub>			
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )			
Continuous current through V <sub>CC</sub> or GND			±70 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: D package	′	113°C/W
	DW package	′	105°C/W
	N package		78°C/W
Storage temperature range, T <sub>sta</sub>		-65°C 1	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### recommended operating conditions

			SN	54HC590	)A	SN74HC590A			UNIT
			MIN	IN NOM MAX		MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V <sub>CC</sub> = 2 V	1.5			1.5			
٧ <sub>IH</sub>	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V
		V <sub>CC</sub> = 6 V	4.2			4.2			
		V <sub>CC</sub> = 2 V	0		0.5	0		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 4.5 V	0		1.35	0		1.35	V
		V <sub>CC</sub> = 6 V	0		1.8	0		1.8	
VI	Input voltage		0		VCC	0		VCC	V
٧o	Output voltage		0		VCC	0		VCC	V
		V <sub>CC</sub> = 2 V	0		1000	0		1000	
t <sub>t</sub> ‡	Input transition (rise and fall) time	V <sub>CC</sub> = 4.5 V	0		500	0		500	ns
		V <sub>CC</sub> = 6 V	0		400	0		400	
TA	Operating free-air temperature		-55		125	-40		85	°C

<sup>‡</sup> If this device is used in the threshold region (from V<sub>IL</sub>max = 0.5 V to V<sub>IH</sub>min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	RAMETER TEST CONDITIONS		V	Т	A = 25°C	;	SN54H	C590A	SN74H	C590A	UNIT
PARAMETER	IES	CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2 V	1.9	1.998		1.9		1.9		
		I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
Voн	$V_I = V_{IH} \text{ or } V_{IL}$	$\overline{RCO}$ , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		V
		$Q_A-Q_H$ , $I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$\overline{RCO}$ , $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
		$Q_{A}-Q_{H}$ , $I_{OH} = -7.8 \text{ mA}$	l o v	5.48	5.8		5.2		5.34		
		⊢	2 V		0.002	0.1		0.1		0.1	
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
VOL	$V_I = V_{IH} \text{ or } V_{IL}$	RCO, I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	V
		$Q_A-Q_H$ , $I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		RCO, I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		$Q_A-Q_H$ , $I_{OL} = 7.8 \text{ mA}$	O V		0.15	0.26		0.4		0.33	
ΙΙ	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	VO = VCC or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

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#### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T <sub>A</sub> =	25°C	SN54H	C590A	A SN74HC590A		LINIT
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	0	4	0	2.5	0	3.2	
fclock	Clock frequency		4.5 V	0	20	0	13		16	MHz
			6 V	0	24	0	16	0	19	
			2 V	125		200		155		
		CCLK or RCLK high or low	4.5 V	25		38		31		
	Pulse duration		6 V	21		32		26		20
t <sub>W</sub>	Fuise duration		2 V	100		150		125		ns
		CCLR low	4.5 V	20		30		25		
			6 V	17		26		21		
			2 V	100		150		125		
		CCKEN low before CCLK↑	4.5 V	20		30		25		
			6 V	17		26		21		
			2 V	100		150		125		ns
t <sub>su</sub>	Setup time	CCLR high (inactive) before CCLK↑	4.5 V	20		30		25		
			6 V	17		26		21		
			2 V	100		150		125		
		CCLK↑ before RCLK↑†	4.5 V	20		30		25		
			6 V	17		26	21			
			2 V	50		75		60		
t <sub>h</sub>	Hold time	CCKEN low after CCLK↑	4.5 V	10		15		12		ns
			6 V	9		13		11		

<sup>†</sup> This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.



# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

					SN54HC590A					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T,	ղ = 25°C	;	MIN	MAX	UNIT	
	(1141 01)	(0011 01)		MIN	TYP	MAX	IVIIIV	WAX		
			2 V	4	8		2.5			
f <sub>max</sub>			4.5 V	20	35		13		MHz	
			6 V	24	40		16			
			2 V		80	150		225		
t <sub>pd</sub>	CCLK↑	RCO	4.5 V		20	31		45	ns	
			6 V		15	26		38		
			2 V		70	130		195		
t <sub>PLH</sub>	CCLR↓	RCO	4.5 V		18	28		39	ns	
			6 V		14	23		33		
	RCLK↑	Q	2 V		70	140		210	ns	
t <sub>pd</sub>			4.5 V		18	31		42		
			6 V		14	25		36		
			2 V		80	125		185		
ten	ŌE↓	Q	4.5 V		20	30		37	ns	
			6 V		15	28		31		
			2 V		80	125		185		
t <sub>dis</sub>	ŌĒ↑	Q	4.5 V		20	30		37	ns	
			6 V		15	28		31		
			2 V		38	75		110		
		RCO	4.5 V		8	15		22		
t <sub>t</sub> *			6 V		6	13		19	ne	
<sup>lt</sup>	тŧ		2 V		38	60		90	ns	
		Q	4.5 V		8	12		18		
			6 V		6	10		15		

<sup>\*</sup> This parameter is not production tested for the SN54HC590A.

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# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

					SN74HC590A					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	v <sub>cc</sub>	T,	λ = 25°C	;	MAINI	MAY	UNIT	
	(INFOT)	(001F01)		MIN	TYP	MAX	MIN	MAX		
			2 V	4	8		3.2			
f <sub>max</sub>			4.5 V	20	35		16		MHz	
			6 V	24	40		19			
			2 V		80	150		190		
<sup>t</sup> pd	CCLK↑	RCO	4.5 V		20	30		38	ns	
			6 V		15	26		33		
			2 V		70	130		165		
<sup>t</sup> PLH	CCLR↓	RCO	4.5 V		18	26		33	ns	
		6 V		14	22		28			
				2 V		70	140		175	
<sup>t</sup> pd	RCLK↑	Q	4.5 V		18	28		35	ns	
·			6 V		14	24		30		
			2 V		80	125		155		
t <sub>en</sub>	ŌE↓	Q	4.5 V		20	25		31	ns	
			6 V		15	21		26		
			2 V		80	125		155		
<sup>t</sup> dis	ŌĒ↑	Q	4.5 V		20	25		31	ns	
			6 V		15	21		26		
			2 V		38	75		95		
		RCO	4.5 V		8	15		19		
, l			6 V		6	13		16	1	
t <sub>t</sub>			2 V		38	60		75	ns	
		Q	4.5 V		8	12		15		
			6 V		6	10		13		

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# switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

	EDOM TO						SN	54HC59	0A		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc	Τ <sub>Δ</sub>	√ = 25°C	;	MIN	MAX	UNIT		
	(1141 01)	(0011 01)		MIN	TYP	MAX	IVIIIV	WAX			
			2 V		100	300		447			
t <sub>pd</sub>	RCLK↑	Q	4.5 V		24	60		90	ns		
			6 V		20	51		77			
			2 V		90	200		300			
t <sub>en</sub>	ŌĒ	Q	4.5 V		23	40		60	ns		
			6 V		19	34		51			
			2 V		45	210		315			
t <sub>t</sub> *		Q	4.5 V		17	42		63	ns		
			6 V		13	36		53			

<sup>\*</sup> This parameter is not production tested for the SN54HC590A.

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

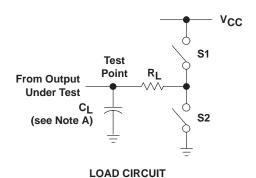
					SN	74HC59	0A			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T	√ = 25°C	;	MIN	MAX	UNIT	
	(1111 01)	(0011 01)		MIN	TYP	MAX	IVIIIV	WAX		
			2 V		100	300		380		
t <sub>pd</sub>	RCLK↑	Q	4.5 V		24	60		76	ns	
				6 V		20	51		65	
			2 V		90	200		250		
t <sub>en</sub>	ŌĒ	Q	4.5 V		23	40		50	ns	
			6 V		19	34		43		
			2 V		45	210		265		
t <sub>t</sub>		Q	4.5 V		17	42		53	ns	
			6 V		13	36		45		

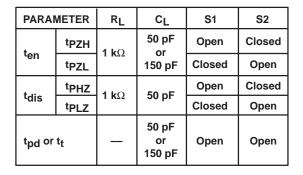
# operating characteristics, $T_A = 25^{\circ}C$

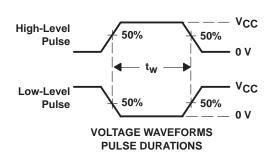
	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	250	pF

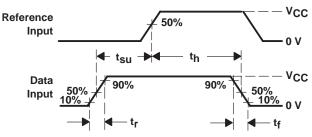


#### PARAMETER MEASUREMENT INFORMATION

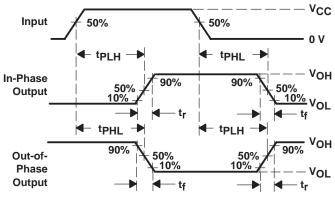


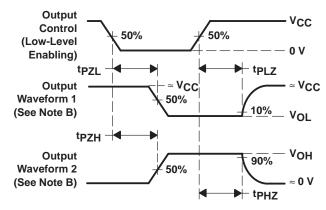






VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES





VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub> = 6 ns, t<sub>f</sub> = 6 ns.
- D. For clock inputs, f<sub>max</sub> is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLZ and tpHZ are the same as tdis.
- G. tpZL and tpZH are the same as ten.
- H. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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